REMARKS

Claims 1, 2, 4, 14, 15, 18 and 19 are pending. The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments and remarks.

Claims 1, 2, 4, 14, 15 and 18 have been rejected under 35 U.S.C. 103(a) as being anticipated by Iwamoto (USPN 6,292,040) in view of McCune (USPN 5,306,971) and further in view of Kunanayagam et al. (USPN 6,850,106). The Examiner stated essentially that the combined teachings of Iwamoto, McCune and Kunanayagam teach or suggest all the limitations of Claims 1, 2, 4, 14, 15 and 18.

Claim 1 claims, *inter alia*, "a delay line, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance, to vary the unit time delay." Claim 14 claims, *inter alia*, "a delay unit, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal and generating the output clock signal in synchronization with the external clock signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance, to vary the unit time delay."

Iwamoto teaches a delay line having delay units controlled by control signals for determining a delay (see col. 2, lines 1-5). Iwamoto does not teach or suggest a delay unit "comprising a plurality of delay cells having various unit time delays…" "wherein each delay

cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance" essentially as claimed in Claims 1 and 14. The delay lines of Iwamoto include delay units Ux comprising inverter circuits (see FIG. 18), each delay unit corresponding a unit for delay adjustment. Iwamoto's unit for delay is not varied. Thus, Iwamoto does not teach or suggest a delay unit including a plurality of delay cells having various unit time delays, much less resistors of a plurality of delay cells having different resistances, essentially as claimed in claims 1 and 14. Therefore, Iwamoto fails to teach all the limitations of Claims 1 and 14.

McCune teaches a delay line comprising gates having multiple delays, including an intrinsic propagation delay t and a longer propagation delay τ (see col. 3, lines 1-5). McCune does not teach or suggest a delay unit "comprising a plurality of delay cells having various unit time delays…" "wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance" essentially as claimed in Claims 1 and 14. McCune teaches that the time delay of a gate is proportional to the capacitive loads applied to the bases of transistors Q1 and Q2 by transistors Q15 and Q 16 (see col. 5, lines 56-58) and further that "by appropriately choosing the number of transistors Q15 and Q 16 in each stage, the delay characteristics of the stage may be controlled" (see col. 5, lines 37-40). Indeed, the intrinsic propagation delay t of the gates are equal, such that $t_1=t_2=t_3$ (see col. 3, line 35). Thus, since the intrinsic propagation delay of each gate is equal, it can be surmised that the resistors of each gate have the same resistance. The delay characteristic being controlled solely by the number of transistors Q15 and Q 16.

Further, the claimed invention discloses that the resistance of resistor R1 in a first delay cell is different from the resistance of resistor R2 in a second delay cell. However, McCune does

not disclose that the resistors R1~R4 of a first gate G1 have different resistances from the resistors R1~R4 of second gate G2.

For the foregoing reasons, McCune fails to teach or suggest that resistors of each gate have different resistances to give various unit time delays, essentially as claimed in Claims 1 and 14. For at least the foregoing reasons, McCune fails to cure the deficiencies of Iwamoto.

Kunanayagam teaches a differential amplifier with resistive loads to implement a single delay cell (see FIG. 2). Kunanayagam does not teach or suggest a delay unit "comprising a plurality of delay cells having various unit time delays…" "wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance" essentially as claimed in Claims 1 and 14. Nowhere does Kunanayagam teach or suggest different differential amplifiers of a delay line having resistors of different resistances, essentially as claimed in Claims 1 and 14. Therefore, Kunanayagam fails to cure the deficiencies of Iwamoto and McCune.

The combined teachings of Iwamoto, McCune and Kunanayagam teach a delay line comprising gates arranged from a least delay to a greatest delay, the delays determined by capacitive load of transistors. The combined teachings of Iwamoto, McCune and Kunanayagam fail to teach or suggest a delay unit "comprising a plurality of delay cells having various unit time delays…" "wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance" essentially as claimed in Claims 1 and 14 (Emphasis added). Therefore, Claims 1 and 14 are believed to be allowable over the combined teachings of Iwamoto, McCune and Kunanayagam.

Claims 2-4 and 15 depend from claims 1 and 14, respectively. The dependent claims are believed to be allowable for at least the reasons given for Claims 1 and 14.

New Claim 19 is believed to be allowable over the cited art.

Claim 19 claims, *inter alia*, "a delay line, comprising a plurality of delay blocks, each delay block comprising a plurality of delay cells having the same unit time delay, wherein the unit time delay of delay cells from different delay blocks are different, the delay line for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistors of the delay cells from different delay blocks have different resistances and the resistors of the delay cells from the same delay block have the same resistance, to vary the unit time delay."

The cited art is not believed to teach or suggest delay blocks, wherein each delay block comprises a plurality of delay cells having the same unit time delay, wherein the unit time delay of delay cells from different delay blocks are different. Therefore, Claim 19 is believed to be in condition for allowance.

For the forgoing reasons, the application, including Claims 1, 2, 4, 14, 15, 18 and 19, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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